Abstract of the Disclosure

An improved memory device and architecture has been detailed that enhances a Flash memory device that has an SDRAM compatible interface. The memory device employs a virtual paging scheme that allows for the architecture of the memory to implement an efficient Flash memory structure internally. Externally, the memory logically maps the internal Flash architecture to an SDRAM compatible interface and virtual architecture, allowing for memory access and operation with a compatible SDRAM controller device. A double data rate interface is provided to allow data to be input and output from the memory in synchronization with both rising and falling edges of a clock signal.